REMARKS

Claims 7-10 are currently pending and stand rejected under 35 U.S.C. § 103(a) as obvious from Castellano in view of Kao. Claims 1-6 were previously cancelled without prejudice.

Claim 7 recites, among other limitations, "a first Gray code to binary converter for generating the particular address indicated by the read pointer; a second Gray code to binary converter for generating the another particular address indicated by the write pointer". Examiner has indicated that Castellano does not teach the foregoing. Examiner has indicated that "Sequential addresses are most suitable when sequential data is to be stored in consecutive addresses in the FIFO, because the addressing schemes used by computer systems are mostly linear, continuous address assignment. Therefore, it would have been obvious for one or ordinary skill in the art at the time of Applicants' invention to use a first Gray code to binary converter for generating the particular address indicated by the read pointer and a second Gray code to binary converter for generating the particular address indicated by the write pointer, as demonstrated by Kao, and to incorporate it into the existing apparatus disclosed by Castellano, to support a linear, continuous address scheme employed by most computer systems."

Assignee respectfully traverses the rejection because Castellano teaches away from this. Assignee calls Examiner's attention to Castellano, Col. 3, Lines 35-45:

> If the counters 18 and 20 were to be implemented as conventional sequential counters, multiple address bit positions could change with each successive increment. When such a counter is sampled with an asynchronous clock (that is, read counter sampled with write clock or write counter sampled with read clock), bogus values can be obtained.
> Accordingly, in a preferred embodiment of the invention, the write counter 18 and read counter 20 are implemented as Gray code counters. In a Gray code counter, no more than one address bit position changes for each increment.

Given Castellano's teaching that with "conventional sequential counters" "bogus values can be obtained", Assignee submits that it would not have been obvious to one of ordinary skill in the art to modify Castellano as suggested by Examiner.

Moreover, Castellano notes that "bogus values can be obtained" when "multiple address bit positions could change with each successive increment". The reason to use a Gray code counter, is because "In a Gray code counter, no more than one address bit position changes for each increment." If "Sequential addresses are most suitable", i.e., "multiple bit positions could change with each successive increment" was acceptable, Castellano's reason for using Gray code would be void. Thus, one skilled in the art would not use Castellano's Gray code, at all, if sequential codes were most suitable.

Accordingly, for at least the foregoing reasons, Assignee respectfully traverses the rejection to claim 7 and dependent claims 8-10.

CONCLUSION

Assignee respectfully submits that each of the pending claims are allowable, making the application in a condition for allowance. Examiner is respectfully requested to pass this case to issuance.

The Commissioner is hereby authorized to charge any deficiency in the amount enclosed or any additional fees which may be required under 37 CFR 1.16 or 1.17 to Deposit Account No. 13-0017 in the name of McAndrews, Held & Malloy, Ltd.

RESPECTFULLY SUBMITTED,

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